PERFORMANCE ANALYSIS OF THE QUANTUM PROCESSOR: BASED ON REVERSIBLE SHIFT REGISTER USING QCA

Rajinder Tiwari
Research Scholar, Department of ECE, ASET, Amity University, Lucknow (India).
Associate Professor, Department of ECE, Model Institute of Engineering and Technology (MIET), Jammu, (India).
E-mail: trajan@rediffmail.com ORCID: https://orcid.org/0000-0003-1734-5892

Anil Kumar
Asst. Pro VC and Director, ASET, Amity University, Lucknow, (India).
E-mail: akumar3@lko.amity.edu ORCID: https://orcid.org/0000-0001-8976-3642

Preeta Sharan
Professor, Department of ECE, The Oxford College of Engineering and Technology, Bengaluru, (India).
E-mail: sharan.preeta@gmail.com ORCID: https://orcid.org/0000-0002-3549-7147

Recepción: 17/12/2019 **Aceptación:** 27/02/2020 **Publicación:** 30/04/2020

Citación sugerida Suggested citation

Tiwari, R., Kumar, A., y Sharan, P. (2020). Performance analysis of the quantum processor: based on reversible shift register using QCA. *3C Tecnología. Glosas de innovación aplicadas a la pyme. Edición Especial, Abril 2020,* 75-91. http://doi.org/10.17993/3ctecno.2020.specialissue5.75-91

ABSTRACT

The concept of the reversible logic depends on the dominant modules of a processor that has motivated to obtain the performance analysis of the quantum based processors. In continuation to this discussion, the shift register can be studied with the use of the reversible logic which is capable of shifting the bits of the information towards both side i.e. left and right. In this process of the analysis of the quantum processor, the Quantum Computational Automata (QCA) as well as Verilog, software has been used so as to simulate the parameters of the device and then obtain the characteristics of the device. In this discussion, a reversible logical computing based approach has been mentioned that can be used in the ALU of a quantum processor with the help of D-type FFs or its combination that act as an inevitable and the most crucial basic building block in the design of quantum processor. This circuit has been designed and analyzed for the most dominant parameters, say, size of cell, number of cells used, delay, temperature dependency, power dissipation, etc. This proposed circuit which acts as an alternative to the CMOS technology, has been analyzed for a typical range of the power dissipation (650 – 750 meV), temperature range (1°K – 10°K).

KEYWORDS

QCA, CMOS, Power Dissipation, QCA Well, Shift Register, Reversible Logic Computation, Quantum Processor.

http://doi.org/10.17993/3ctecno.2020.specialissue5.75-91

1. INTRODUCTION

The QCA is the foremost and potentially promising technology which has been accepted for the typical Nano range of the frequency in the device implementations. In other words, we can say that this QCA has been emerged as the solution to the limitations of the CMOS Technology existing in the range of microns or micro of the frequency i.e. in terms of speed or delay of the data transmission, density or area in terms of the number of quantum cell used, etc. Due to this unique feature of the quantum computing with the help of QCA has emerged as a fantastic approach in the design and implementation of the device that provides the desired characteristics and performance. The demonstration of the QCA technology has been done simply by implementing it with Quantum Dots i.e. metal dots at quite predominant range of the parameters, say, temperature, pressure, etc. (Tiwari, Kumar, & Sharan, 2018).

It means that these metal dots have been used in the design of various basic blocks or modules of this system such as QCA based wires, logic gates, memories, and reversible gates. As per Moore's law, it has been seen that after every ten years the density of the components fabricated on the chip gets almost doubled that becomes the most significant limitations of the CMOS Technology. In other words, it has been observed that size and area of the fabricated board keeps on increasing that in turn increases the overall size of the processor. Due to this reason, the power dissipation i.e. loss of energy is quite large in this technology, delay is also quite huge. All these limitations are taken care by simply making use of QCA tools that operate in the range of nanoscale. In this technology, the fabrication techniques of the chips played quite dominant role with the desired performance such as preparation of dyes for the ICs which includes quite complex structure and resistant to various degradation methods. The fabrication process of the ICs includes the standard techniques as compared to the conventional methods of separating the impurities such as oxidation, membrane separation, precipitation, etc. (Tiwari *et al.*, 2018).

An important problem of the design and implementation of reversible logic based universal shift register for a quantum processor, especially, the ALU of desired bit. In the context of designing the highly efficient ALU, one must formulate the study and implementation of the important modules of the ALU such as comparator, shift register, logic gates, memories, etc.

http://doi.org/10.17993/3ctecno.2020.specialissue5.75-91

with the help of the reversible computing. In this discussion, the problem has been based on designing and implementing a reversible logic based shift register that is bidirectional in nature. Now in order to obtain the understanding of this technique, one must obtain the comparative analysis of this concept with the prevailing technology i.e. CMOS Technology. For the proper understanding of this technology, one must discuss the development process of this technique with the help of ITRS in the scale of 45nm (Tiwari *et al.*, 2017).

2. QUANTUM CELLULAR AUTOMATA (QCA)

With the development of this technology in the nano scale range, various devices have been designed and implemented which in turn becomes the basic building blocks of most of the system, say, ALU which is designed for quantum processors. Few of the most commonly used devices based on this system are discussed below with help of figures. It is commonly used in the circuits based on nano technology i.e. in nanometer scale with an innovative feature of bonding the charge carriers in more than one dimension. In this topology, the charges are contained in this circuit due to its potential energy. The typical examples of the quantum dots are shown in the below Figure 1 (b) (Tiwari *et al.*, 2018).

The basic logical unit which behaves as the most commonly used element in the quantum computational automata (QCA) as shown in below Figure 1 (a). On the basis of the performances and results obtained with the use of this device i.e. QCA in nanoscale of the frequency of the input signal as compared to the 45 nm CMOS technology. This technology has proved to be the best alternative of the devices like the transistors, silicon, and CMOS paradigm with the quantum elements i.e. QCA well of quantum energy (Tiwari, 2019).

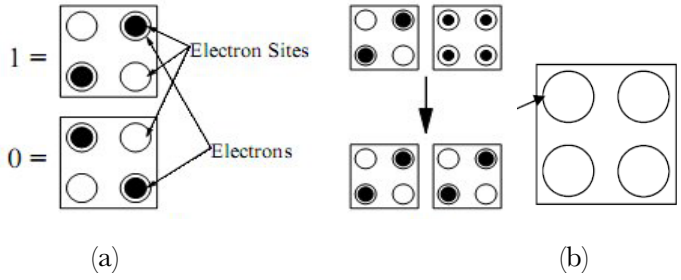

Figure 1. (a) QCA (b) Single Cell. Source: (Tiwari *et al.*, 2018).

http://doi.org/10.17993/3ctecno.2020.specialissue5.75-91

The quantum computing is implemented simply by controlling the tunneling phenomenon of the charges with the help of four phase clock signal of the cell that has been used in the development of the system as shown in the below Figure 2 (Singh, & Pandey, 2016).

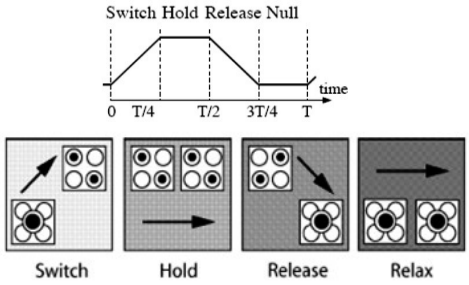

Figure 2. QCA Clockwise Sequencing. Source: (Tiwari *et al.*, 2018).

QCA Wires as shown in below Figure 3.

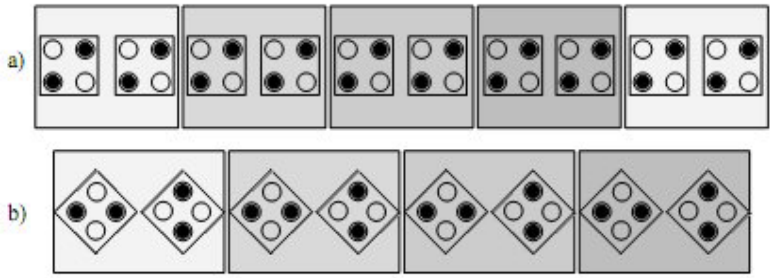

Figure 3. (a) 90° Orientation (b) 45° Orientation of the Cell. Source: (Tiwari *et al.*, 2018).

Majority gate i.e. a three inputs A, B and C device using fours quantum cells as shown in below Figure 4. These cells are oriented with the charge orientation based logic values i.e. 0 and 1with the corresponding input and out terminals. The operational behavior of this majority has been explained with the help of below given equation 1 (Thapliyal, Ranganathan, & Kotiyal, 2013).

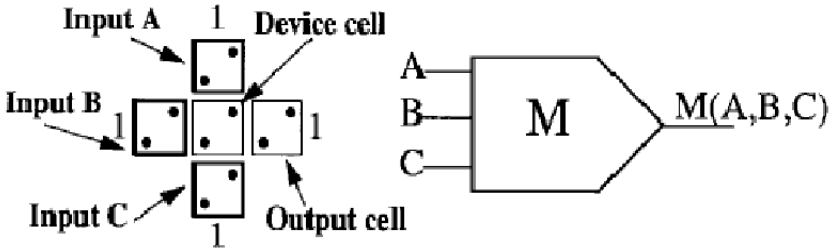

Figure 4. M-Gate. Source: (Rajmohan, & Ranganathan, 2011).

http://doi.org/10.17993/3ctecno.2020.specialissue5.75-91

$$M(A,B,C) = AB + AC + BC \tag{1}$$

Logical gates as shown in below Figure 5.

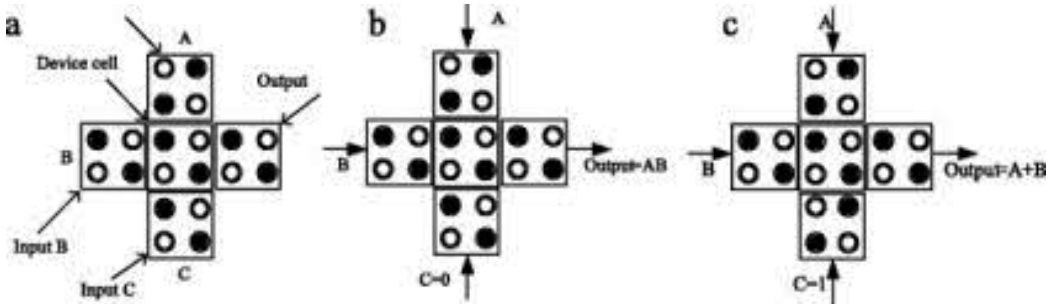

Figure 5. Logic Gates using QCA. Source: (Ganesh, Kishore, & Rangachar, 2008).

QCA Based Memories as shown in the below given Figure 6.

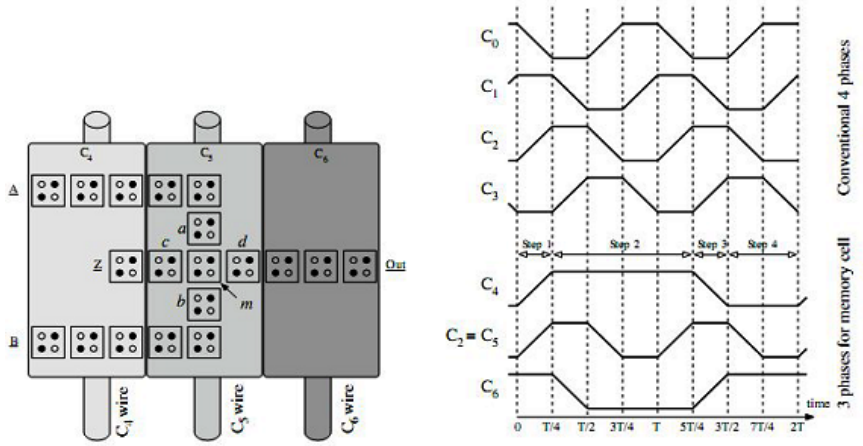

Figure 6. Line based QCA Memory. Source: (Ganesh *et al.*, 2008).

These gates operating on reversible computing have equal number of inputs and outputs as compared to the traditional gates and have bi-mappings between input vectors and output vectors; consequently the input data can be recreated from the output vector states. A reversible gate with n inputs and n output is known as n * n gate as shown in below Figure 7. Feynman Gate is a 2 * 2 reversible gate as shown in the below Figure 7 which is also known as CNOT, i.e., controlled NOT Gate. The input (A, B) and output (P, Q) relation is as follows i.e. (Roohi & Khaemol, 2014).

http://doi.org/10.17993/3ctecno.2020.specialissue5.75-91

$$P = A \tag{2}$$

$$Q = A \oplus B \tag{3}$$

On the contrary, Fredkin gate is a (3 * 3) conservative reversible gate as shown in the below Figure 8. The relation between input vectors and its output vectors is as follows (Walus *et al.*, 2004).

$$P = A \tag{4}$$

$$Q = \bar{}AB + AC \tag{5}$$

$$R = AB + \bar{}AC \tag{6}$$

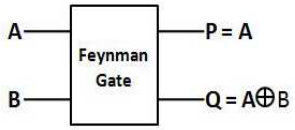

Figure 7. Feynman Gate. Source: (Ali, Hossin, & Ullah 2011).

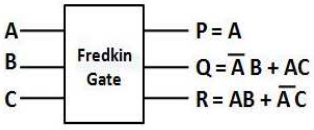

Figure 8. Fredkin Gate. Source: (Ali, Hossin, & Ullah 2011).

3. REVERSIBLE COMPUTING BASED SHIFT REGISTER MEMORY

Based on the above discussion about the performance of the reversible logic based gates as compared to the traditional gates, there are ample circuits that have been implemented for the quantum system. Out of these, the author has discussed the behavior of the shift register based memory cell which proves to be the most valuable module of the quantum processors. The typical design of the memory cell i.e. shift register is shown in the above given Figure 9 (Tiwari *et al.*, 2017).

http://doi.org/10.17993/3ctecno.2020.specialissue5.75-91

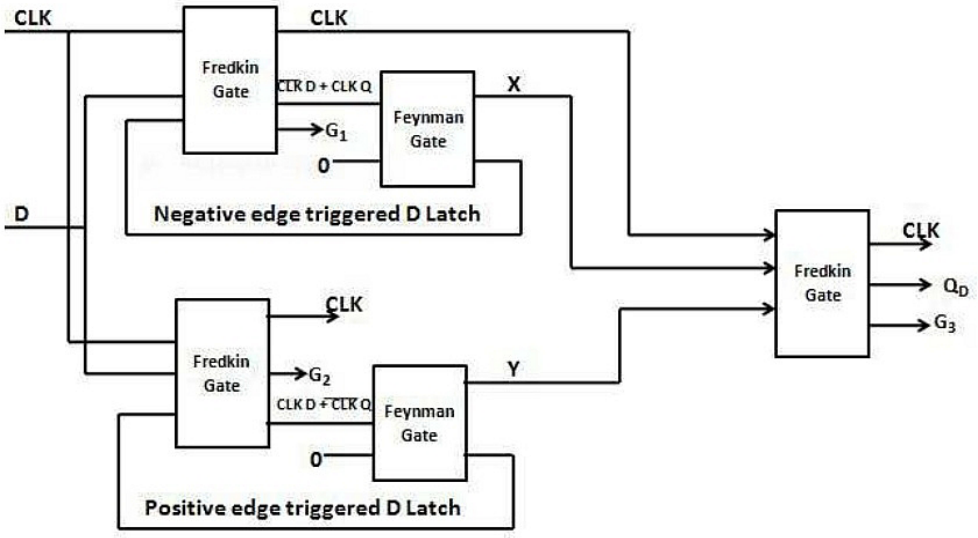

Figure 9. Basic Diagram of Shift Register Memory. Source: (Das & De, 2013).

$$X = \left(\left(R/W \right)' .D + \left(R/W \right) D' \right) = X \odot D \tag{7}$$

$$Y = D \tag{8}$$

4. PROPOSED UNIVERSAL SHIFT REGISTER MODEL FOR QUANTUM PROCESSORS

Reversible Universal Shift Register for Quantum Processor (ALU):

In this discussion, the author has extended the above discussion of designing and implementing the shift registers which is capable of rotating in both left and right direction with the reversible logic gates. In this discussion, reversible computing based Delay Flip Flop and 4:1 multiplexer has been used to obtain the circuit design. The efficiency of this proposed circuit has been evaluated using QCA and an analysis can be obtained with the reference circuit based on the number of cell i.e. density of the circuit, data transferring speed i.e. delay, etc. The below given 10 and 11 shows the design of the circuit using the QCA tool. Here the Figure 10 shows 4-bit shift register which has been design by making use of 4:1 MUX and four stages of the Delay Flip Flop with the PIPO data flow. Similarly, the below given Figure 11 provides us an alternative approach of the design of

http://doi.org/10.17993/3ctecno.2020.specialissue5.75-91

the proposed circuit with the help of the reversible gates i.e. 8:1 MUX and eight stages of Delay Flip Flops.

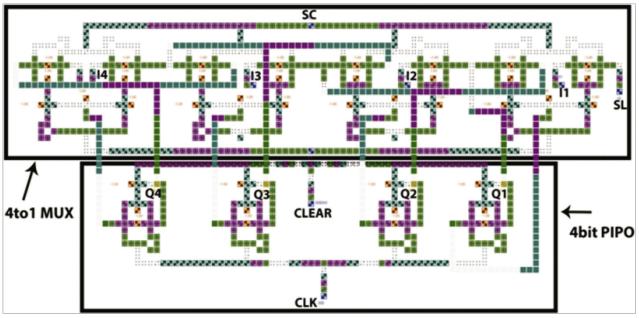

Figure 10. Proposed Circuit (Universal Shift) PIPO-4-Bit.

Figure 11. Proposed Circuit (Universal Shift) PIPO-8-Bit.

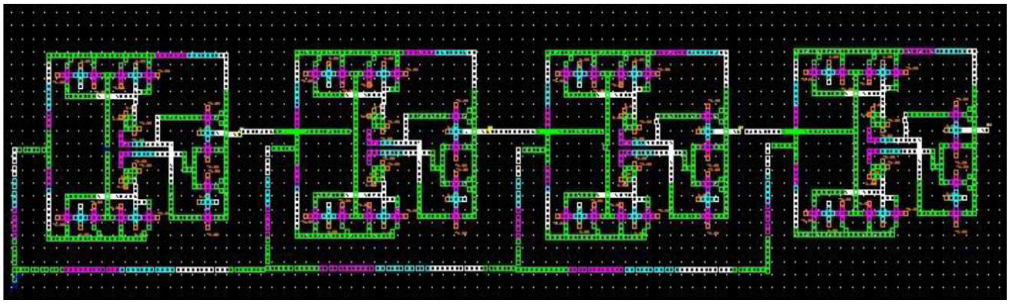

Figure 12. Proposed Circuit (Universal Shift) SIPO 4-Bit.

The above Figure 12 shows another configuration of designing the proposed model with SIPO data flow tendency with the use of Delay Flip Flops.

Reversible Logic Gates Based D Flip Flop:

Another technique of designing the circuit of Delay Flip Flop has been considered for the quantum processors, especially, the modules which are dominant for the design of ALU. The below given Figure 13 shows the Delay Flip Flop using the QCA Designer Tool 2.0.

http://doi.org/10.17993/3ctecno.2020.specialissue5.75-91

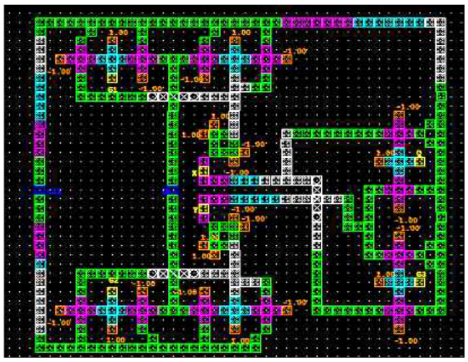

Figure 13. QCA Implementation of D Flip Flop used in Proposed Circuit.

Reversible 4:1 Multiplexer Using QCA Tool:

The below given Figure 14 (a) and 14 (b) shows the schematic arrangement of the 4:1 MUX so as to obtain the desired performance in terms of switching the desired input at the output of the circuit. This circuit has been proven to the most predominant module of the shift register of the ALU designed primarily for the quantum processors.

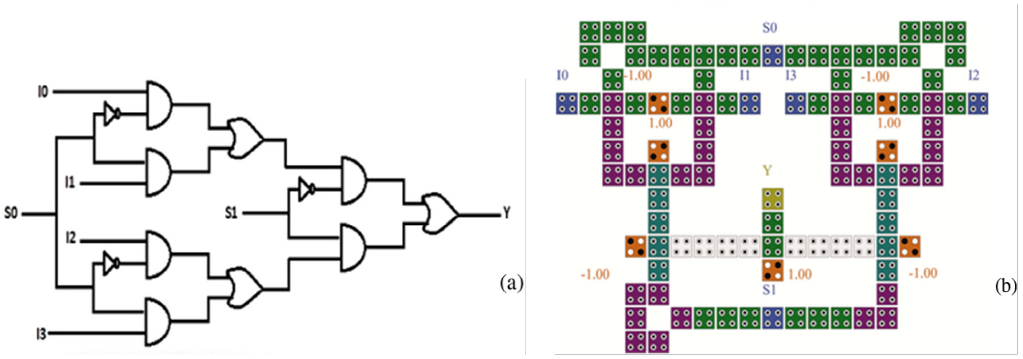

Figure 14. Schematic Circuit & QCA Implementation of 4: 1 MUX used in Proposed Circuit.

5. SIMULATION RESULTS & DISCUSSIONS

The performance of the proposed model discussed based on the most pre-dominant parameters of the reversible logic based shift register i.e. area of the cell, number of cells used, delay i.e. speed of the data transmission between output and input of the circuit. Thus, based on the behavior of these parameters, using QCA Designer Tool 2.0, writing the codes for the structure behavior of the proposed model using VHDL and Verilog codes. In this proposed circuit, the author has made the use of the reversible gates with best

http://doi.org/10.17993/3ctecno.2020.specialissue5.75-91

efficiency i.e. Fredkin & Feynman gates. From this simulation as shown in Figure 15, it has been observed that the power dissipation or the loss of information of these two reversible gates is quite less as compared to others. Due to this reason, these gates are quite common in use for the development of various modules of the quantum processors. These reversible gates have got a limitation due to tunneling effect of the energy which in turn causes the increase in the power dissipation. This discussion of the author has been supported with the help of below give Table 1 and Figure 16 that gives the information of the power dissipation of the proposed model with respect to the circuits of the reference work done by others.

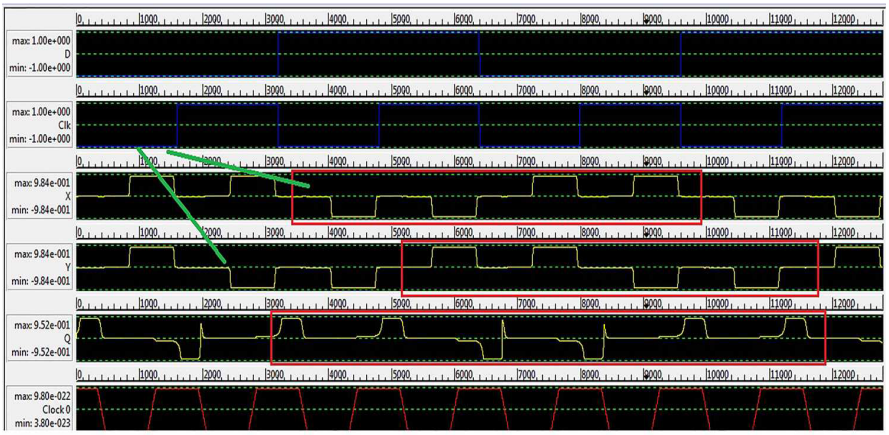

Figure 15. Simulation results of the Proposed Circuit using QCA Designer Tool.

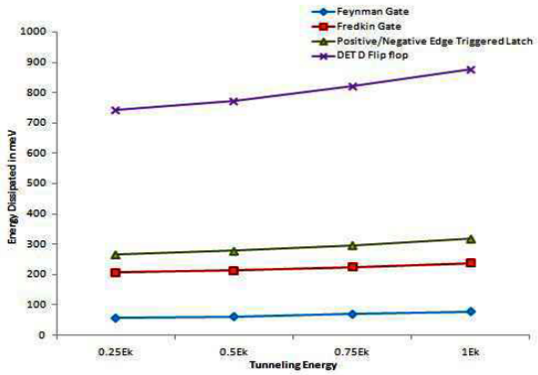

Figure 16. Power & Energy Analysis of the Proposed Model.

This discussion based on the performance of the proposed circuit of universal shift register has been carried out based on the delay comparison, cell count comparison, area comparison has been simulated with the use of some suitable software as shown in below Figure 17.

http://doi.org/10.17993/3ctecno.2020.specialissue5.75-91

Table 1. Power Dissipation in Proposed Model using Reversible Logic Gates.

Proposed QCA Based Model	Power Dissipated at T=2°K (meV)			
	0.25Ek	0.5Ek	0.75Ek	1Ek
Feynman Gate	58.4	63.4	70.9	79.6
Fredkin Gate	208.6	215.6	226.6	239.6
Reversible 4:1 MUX	267	279	297.5	318.8
Reversible D Flip flop	742.6	773.6	821.6	876.8
Reversible Universal Shift Register	651.2	648.2	676.2	688.2

The below given Figure 17 fives the behavior of the universal circuit with the reference work carried out by other researchers in terms of the temperature with a mean polarization of the quantum cells i.e. XE-001 neV.

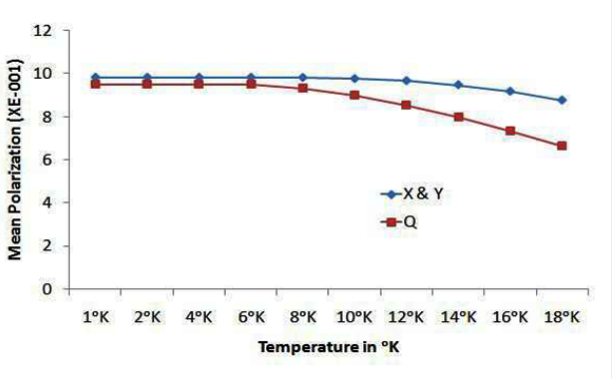

Figure 17. Comparison of the Proposed Model with Reference Model in terms of Temperature.

From the above discussions, it has been found that the power dissipation and the loss of energy of the proposed circuit using majority gates using the reversible computing ability. On this basis of these all, the author has concluded with the simulated result supported by Table 1 providing the comparative analysis based on the considered parameters.

http://doi.org/10.17993/3ctecno.2020.specialissue5.75-91

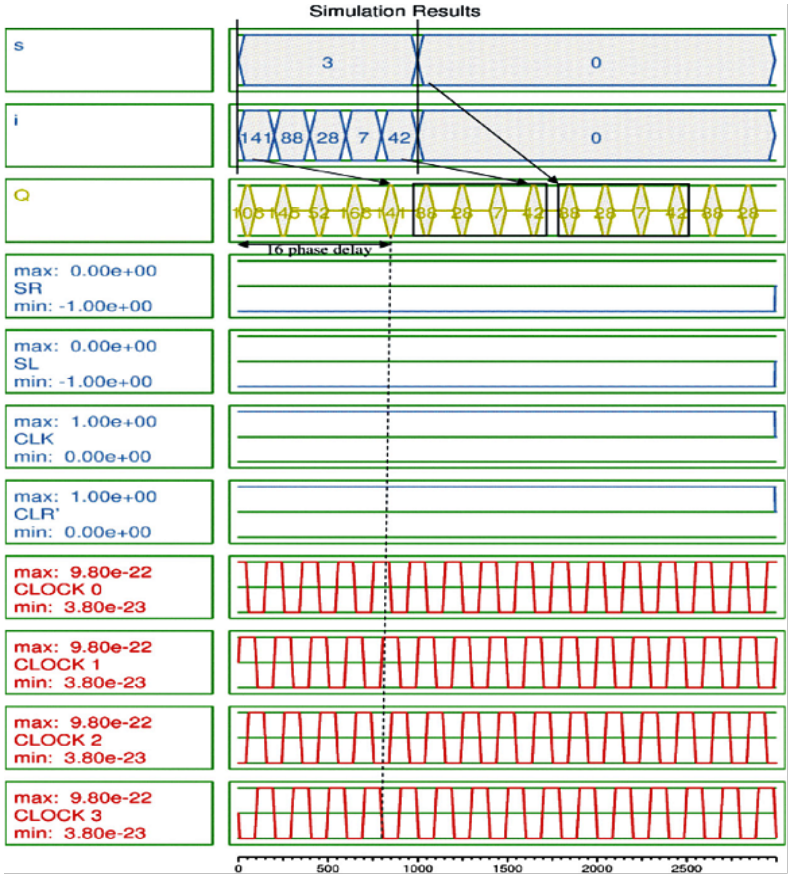

Figure 18. Overall Performance Based Simulation Results of the Proposed Model.

The above Figure 18 shows the overall performance of the proposed model of the universal shift register for the quantum processor, i.e. the ALU which is using the reversible logic based computing as compared to the 45 nm CMOS Technology.

6. CONCLUSION

In this paper, the authors has undergone with a non-exhaustive literature survey to obtain the problem enunciation of this problem. In this process, the author has taken the most dominant parameters i.e. number of cells, delay and area of the quantum cells of the reversible gates to design and implement an innovative circuit of universal shift register that can be used for the design of ALU of the quantum processor. In this context, the author has made the use of the circuit of 4:1 multiplexer in addition to the reversible gate based D

http://doi.org/10.17993/3ctecno.2020.specialissue5.75-91

flip flop in order to design and implement the 4-bit as well as 8-bit shift register with SIPO and PIPO based data transmission. This proposed circuit which acts as an alternative to the CMOS technology, has been analyzed for a typical range of the power dissipation (650-750 meV), temperature range (1°K-10°K).

ACKNOWLEDGEMENTS

The authors are thankful to Hon'ble C-VI (Additional President, RBEF and Chairman AUUP, Lucknow Campus), Maj. Gen. K. K. Ohri, AVSM, Retd. (Ex-Pro VC), Amity University, Lucknow Campus, Prof. (Dr.) Sunil Dhaneshwar, Pro-VC Amity University, Lucknow Campus, Prof. (Dr.) Arun Gupta, Chairman, MIER Group, Dr. Renu Gupta, Vice-Chairman, MIER Group, Prof (Dr.) Ankur Gupta, Director, MIET Jammu, Wg. Cdr. Dr. Anil Kumar, Retd. (Director, ASET), Prof. Preeta Sharan, Professor & Co-Guide, The Oxford College of Engineering, Bengaluru, Mr. Jamini Sharma, HoD, ECE, MIET, Jammu for their support in carrying out the research work efficiently.

REFERENCES

Ali, M. B., Hossin, M. M., & Ullah, M. E. (2011). Design of Reversible Sequential Circuit using Reversible Logic Synthesis. *International Journal of VLSI Design & Communication Systems (VLSICS)*, *2*(4), 37-45. https://www.researchgate.net/publication/276200730_Design_of_Reversible_Sequential_Circuit_Using_Reversible_Logic_Synthesis

Das, J. C., & **De, D.** (2013). Reversible binary to grey and grey to binary code converter using QCA. *IETE Journal of Research, 61*(3), 223–229. https://doi.org/10.1080/03772063.2015.1018845

Ganesh, E. N., Kishore, L., & Rangachar, M. J. S. (2008). Implementation of quantum celular automata combinational and sequential circuits using Majority Logic reduction method, *International Journal Nanotechnology and Applications, 2*(1), 89-106. https://www.academia.edu/8038090/Implementation_of_Quantum_cellular_automata_combinational_and_sequential_circuits_using_Majority_logic_reduction_method

Rajmohan, V., & Ranganathan, V. (2011). Design of Counters using Reversible Logic. In *3rd IEEE International Conference on Electronics Computer Technology*, 138-142. https://doi.org/10.1109/ICECTECH.2011.5941973

Roohi, A., Khademolhosseini, H., Sayedsalehi, S., & Navi, K. (2011). A Novel Architecture for Quantum-Dot Cellular Automata Multiplexer. *International Journal of Computer Science Issue (IJCSI), 8*(6), 55-60. https://www.ijcsi.org/papers/IJCSI-8-6-1-55-60.pdf

Shamsabadi, A. S., Ghahfarokhi, B. S., Zamanifar, K., & Movahedinia, N. (2009). Applying inherent capabilities of quantum-dot cellular autómata to design: D flip flop Case Study. *Journal of System Architectecture, 55*(3), 180–1877. https://doi.org/10.1016/j.sysarc.2008.11.001

Singh, R., & Pandey, M. K. (2016). Design and Optimization of Sequential Counters using a Novel Reversible Gate. In *International Conference on Computing, Communication and Automation, (ICCCA), Noida, India*. https://doi.org/10.1109/CCAA.2016.7813936

Thapliyal, H., Ranganathan, N., & Kotiyal, S. (2013). Design of Testable Reversible Sequential Circuits. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 21(7), 1201-1209. https://doi.org/110.1109/TVLSI.2012.2209688

Tiwari, R. (2019). A Novice Approach to Implementation of System on Chip Based Smart CMOS Sensor for Quantum Computing Based Applications. In *2nd International Conference on Microelectronics, Computing and Communication Systems (MCCS 2017), 476, 563-574.* https://www.researchgate.net/publication/330222760_A_Novice_Approach_to_Implementation_of_System_on_Chip_Based_Smart_CMOS_Sensor_for_Quantum_Computing_Based_Applications

Tiwari, R., Bastawade, D., Sharan, P., & Kumar, A. (2017). Performance Analysis of Reversible ALU in QCA. *Indian Journal of Science & Technology, 10*(29), 01-05. https://www.researchgate.net/publication/319466556_Performance_Analysis_of_Reversible_ALU_in_QCA

http://doi.org/10.17993/3ctecno.2020.specialissue5.75-91

Tiwari, R., Kumar, A., & Sharan, P. (2018). Design and Implementation of 4:1 Multiplexer for Reversible ALU using QCA. In *2nd International Conference Microelectronics and Telecommunication Engineering (ICMETE 2018), Ghaziabad, India,* 191-196. https://doi.org/10.1109/ICMETE.2018.00050

Tiwari, R., Kumar, A., & Sharan, P. (2018). Performance Analysis of Universal Circuit for Reversible ALU using QCA & CMOS Technology. *International Journal of Engineering & Technology (UAE)*, *7*(4.38), 732-736. https://doi.org/10.14419/ijet.v7i4.38.25775

Walus, K., Dysart, T. J., Jullien, G. A., & Budiman, R. A. (2004). QCADesigner: a rapid design and Simulation tool for quantum-dot cellular autómata. *IEEE Transactions on Nanotechnology, 3*(1), 26-31. https://doi.org/10.1109/TNANO.2003.820815

http://doi.org/10.17993/3ctecno.2020.specialissue5.75-91

http://doi.org/10.17993/3ctecno.2020.specialissue5.75-91