DESIGN OF RECONFIGURABLE MEMS-PLL FOR HIGH END TUNING CIRCUITS

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ABSTRACT

The designs of memristive circuits become more demanding since the evaluation of miniaturized models are rapidly increasing every year. Here a novel Memristive Digital Phase locked loop circuit is evaluated. In the existing research works it is found that design of analog domain memristor creates enormous noise and limitations. In the Proposed system, Design of MEMS activated DPLL is evaluated. Digital PLL plays a major role in high-speed communication platforms. The benefits of PLL like jitter free clock generation, stabilized regulation and less resilient is improved even more in MEMS controlled DPLL we call as MEMPLL. In the proposed system an adaptive DPLL vary with respect to Memristor is developed here. The evaluation of memristor emerging in the field of large memory architecture and complex tuning. The advantage of storing the N info at the memristor can vary the development circuits in a reconfigurable manner. Here, the parameters are compared by DCO and ADC method and the power is achieved by 3.0 mw.

KEYWORDS

Memristor, DPLL, Reconfigurable Design, Low power RTL, Clock gating.

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1. INTRODUCTION

Memristor is nothing but a resistor with memory in which the resistance values can be varied which depends upon the amount of electrical charge applied to the programmable emulator (Borghetti *et al.*, 2010). A memristor is a passive two terminal component in which the internal resistance is tunable with respect to the low-level digital clock which we call as memristor control clocks. N combinations of Memristor constants are generated (Chua, 1971). Since all passive devices work with the base of ohms law the parameter variation in memristor can tune the Voltage and current oscillations too (Williams, 2008).

A traditional Phase locked loop system takes a processing time and locking time when the input transition and output stability reachable depends on the tuning factors of the PLL circuitry. Phased detector here we call as delay detector is used to detect the difference in the time period and when comparing with the feedback signal received after the N-Counter (Borghetti *et al.*, 2010).

SYSTEM DESIGN: MODELSIM 6.3 a mentor graphics tool is used to simulate the RTL code whereas XILINX 12.5 is used for FPGA implementation. Architects of digital systems are unavoidably looked with the undertaking of testing their structures. Each design can be made out of numerous parts, every one of which must be tried in disengagement and afterward incorporated into a structure when it works effectively. To confirm that a plan works accurately we utilize simulation, which is a procedure of testing the structure by applying inputs to a circuit and watching its conduct. The output of a simulation is an arrangement of waveforms that indicate how a circuit acts dependent on a given inputs of information sources.

2. MATERIALS AND METHODS

Semiconductor based memristance can be designed by the semiconductor industry, like how they designing the diodes, transistors, inductors, capacitors etc. In our project we are experimentally showing the working of the MEMRISTOR (Strukov *et al.*, 2008) and their few useful applications (Chen *et al.*, 2015). We designed a concept called Memory which is capable of storing the calculated resistance values.

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Calculating resistance values and storing in the Memory.

Initial resistance value to be 100 ohms.

Maximum resistance value to be 10 kilo ohms.

In between a sweep of resistance with an increment step size of 38.66 is added up. That is, default 100 ohms.

If one step increase in input voltage, now resistance value will be 100+38.66 = 138.66 ohms,

If input voltage increased 2 steps, now resistance value will be 100+(38.66 x 2) = 177.32 ohms, like this the resistor values are being calculated and stored in a memory designed using a "n" Bit Multiplexer.

2.1. MEMRISTIVE DPLL

PLL is used to generate a stable oscillating frequency of clock with having the input of any unknown clock with less stability or we call as jittered clock. The ability of PLL to enhance the performance of oscillating when reaching the locking stage helpful to many communications systems and medical equipments depend on the usage of phase locked loop (Li, Mazumder, & Chua, 2004).

General Expression used for Clock Generator:

V upper threshold = (Rmemristor / Rstandard) X Vsat

V lower threshold = - (Rmemristor / Rstandard) X Vsat

Schmitt trigger normally depend on the positive threshold and negative threshold. Variations in memristor tune the Schmitt trigger accordingly.

Where:

Rstandard = any standard resistor value

Rmemristor = Replaced with MEMRISTOR

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Vsat = input constant voltage

So, depends upon the Change in MEMRISTOR Value, the pulse shaping of the memristor getting changed.

2.2. DESIGN DESCRIPTION

2.2.1. DESIGN OF MEMRISTOR

This module is used to design a memristor model using RTL Program. Memristor is a two-terminal element whose resistance depends on the magnitude and direction, and duration of the applied voltage. Hence the voltage inputs are given as low-level configuration bits in the RTL architecture

2.2.2. DESIGN OF MEM-THRESHOLD COMPARATOR

Difference of normal digital comparator and threshold comparator using memristor is evaluated here. Here we design a tunable threshold comparator using memristor. Depends upon the tunable resistance the threshold value of the comparator gets changed. The voltage is passed and hence various pulses produced (Shirinzadeh *et al.*, 2016).

2.2.3. DESIGN OF MEM-DCO

Digitally controlled oscillator circuit is implemented here with the help of tunable memristor. A simple DCO circuit (Testa *et al.*, 2016) is designed using a square wave generator in which the tunable memristor is developed at the feedback of the tuning factor. Hence the square wave signals are varied according to the memristor (Kvatinsky *et al.*, 2013).

2.2.4. DESIGN & INTEGRATION OF MEMPLL

This module is used to integrate the sub modules and finally to produce the accumulated model of Tunable or reconfigurable MEMPLL model using RTL architecture. MEM PLL (Alibart *et al.*, 2012) takes some processing time to reach the locking condition like how the traditional PLL does. Multiple operations and Speed can be varied in accordance to the input variation.

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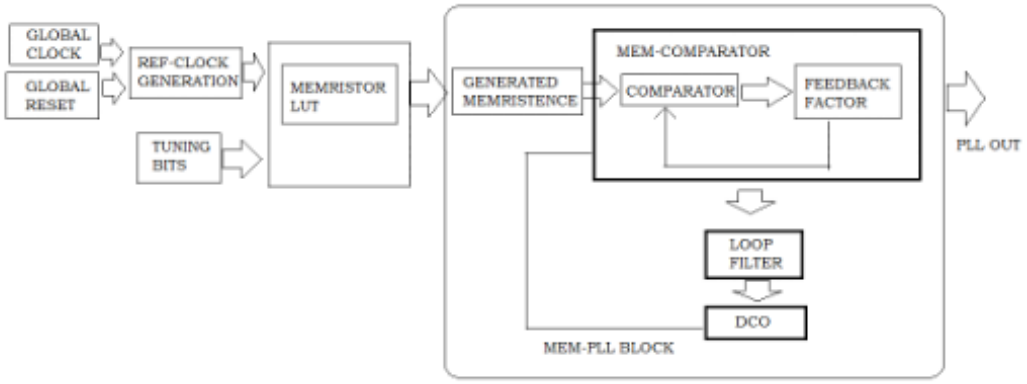

Figure 1. DPLL Existing block diagram.
Source: own elaboration.

2.3. WORKING PRINCIPLE

In any VLSI systems the source clock is normally the global clock generated from the crystal oscillator. The global clock generally called as GCLK is further used to clock tree synthesis (Pickett *et al.*, 2009). Global reset is connected to hardware reset which is active high reset.

2.3.1. REFERENCE CLOCK GENERATOR

A simple clock tree synthesizer is here called as a reference clock generator since reference generators are used to divide the clock, multiply the clock frequency, generate the unique pulses, timing control pulses, etc. (Amarú, Gaillardon, & Micheli, 2014).

2.3.2. TUNING BITS

Memristor is controlled purely through digital configuration bits. Those bits we call as Low level digital tuning pulses. Reconfigurable multiplexer is used for the purpose (Jo et al., 2010).

2.3.3. MEMRISTOR LUT

Look up table generation is another method of temporary register memory. Memristor values are estimated and stored in a configurable LUT which can be easily increased to 2 power N combinations depend upon the future requirements. LUT is also referred as

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sequential mux sometimes; the mux control is synchronized with clock too (Wang *et al.*, 2017).

2.3.4. MEMRISTIVE COMPARATOR

Memristor based comparator is used here to compare the input unknown clock with the reference clock. Depends upon the tuned memristor value the performance of the comparator got changed (Duan et al., 2012).

2.3.5. FEEDBACK FACTOR

When the tunable memristor controls the flow of comparator operation the tunable factor gets changes through the memristor. The output depends upon the tunable factor present in the comparator feedback resistor Rf.

2.3.6 LOOP FILTER

Loop filters are used to remove the noise present in the path of the clock generator. Peak noise is removed through it. A digital filter is used here.

2.3.7. MEMS-DCO

This is an interesting module of MPLL that the tunable comparator result and further fetched to digitally controlled oscillator. The digitally controlled oscillator is synchronized with the memristor value so that the tunable factor is directly proportional to the oscillation capacity of the DCO.

2.3.8. PLL OUTPUT

Ultimately the tunable Memristor controls the majority of DCO operation and Comparator operation which act as key factor for digital PLL locking state. Hence the output produced here will be clearly a stable clock with equal duty cycle and jitter free which can be generated at the output pin of the DPLL after the locking condition occurs (Hu *et al.*, 2012).

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3. RESULTS

3.1. DESIGN OF MEMRISTOR

The below shown result clearly depicts how the memristor tuned by simply applying the digital input in the form of digital bits here we declared as in volt. 4 bit configuration is designed here as a prototypic model (Abdalla & Pickett 2011). The same platform can be used for N number of configurations. 2 power N tunable memristor can be generated. The memristors are usually depicted as artificial intelligence too since we can derive any kind of analog circuit with the help of memristor FPGA combination (Shilpa & Jawahar, 2019; Shilpa, Jawahar, & Karthik, 2018).

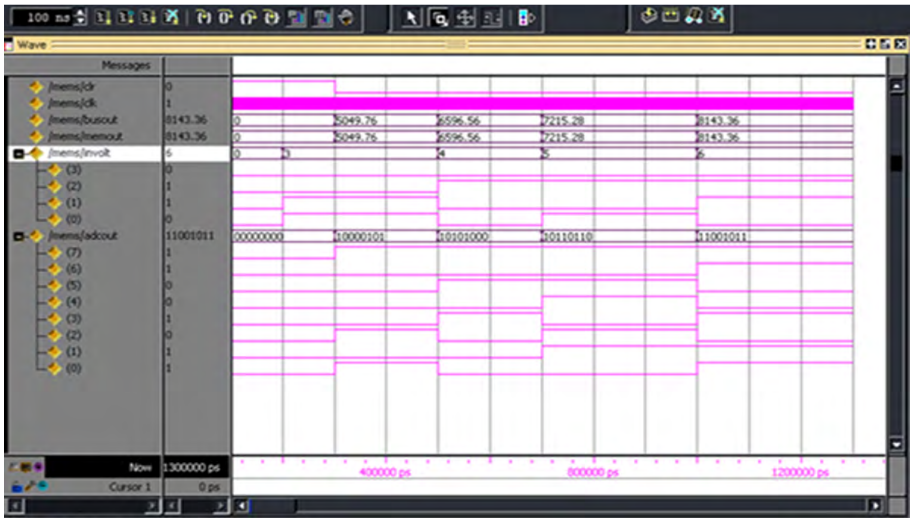

Figure 2. Simulation of Memresistor with 4 binary inputs.
Source: own elaboration.

3.2. SIMULATION RESULT OF PLL USING MEMS

Digital PLL has enormous advantages in communication systems and high-end processing designs. The implemented Tunable DPLL varies in time at every oscillating input which can be purely jitter free and glitch free. Low power techniques such as Clock gating and power gates are used in the behavioural model to design the RTL architecture hassle free (Lee & Mazumder, 2008).

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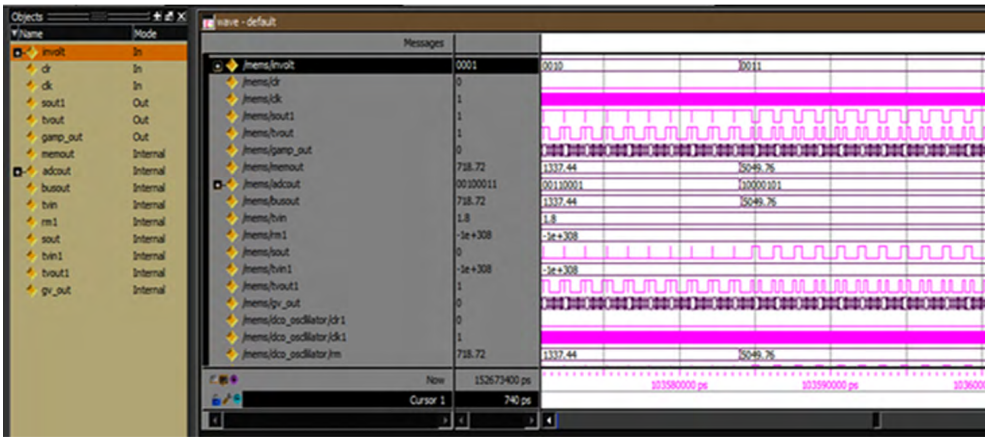

Figure 3. Simulation Result of PLL Using MEMS.
Source: own elaboration.

3.3. SIMULATION RESULT OF PLL TRANSLATION

Traditional PLL takes some sort of clock cycles combined to form a locking time in which the PLL completely stay stabilized. The advantageous MPLL produce less time delay in locking time another important factor is the translation time or the resilient shift of the MEMPLL is clearly depicted in the below simulation result. It takes less <2 clock cycles for resilient shift.

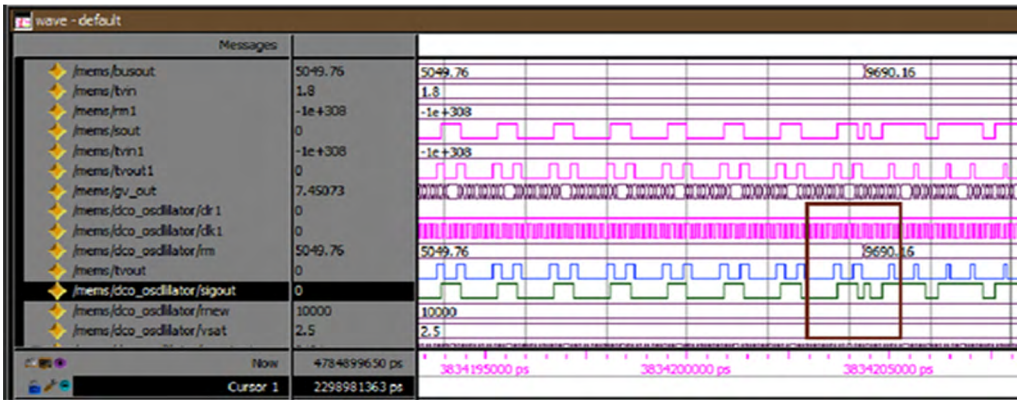

Figure 4. Simulation result of PLL translation.
Source: own elaboration.

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3.4. SCOPE MONITORING OF MEMPLL

The operating frequency of scope will be minimum 100 MHZ henceforth the tunable mem PLL is clearly monitored here.

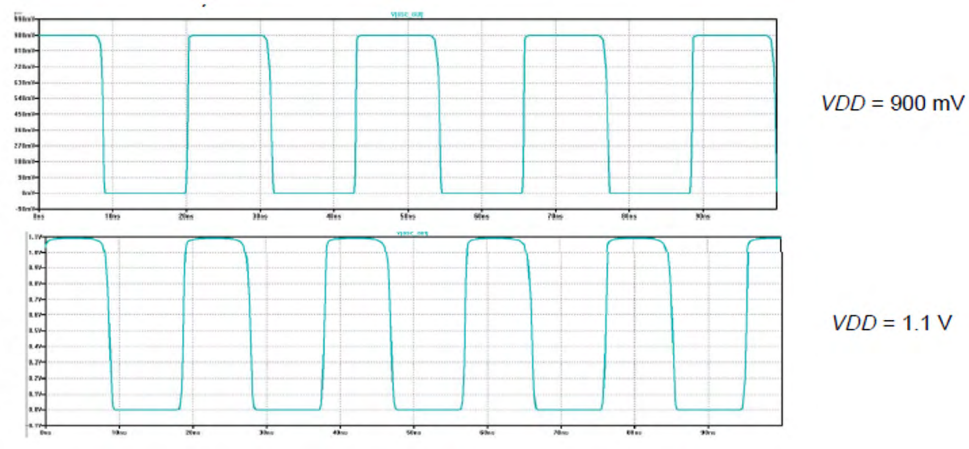

Figure 5. Simulation result OFMEM PLL with their tunable range.
Source: own elaboration.

3.5. COMPARATIVE RESULTS

Table 1. Comparative Result of Traditional PLL with Reconfigurable DPLL.

TOPOLOGY	METHODOLOGY ADC METHOD	ADAPTED DCO METHOD	MEM-PII METHOD
Power supply (V)	+5	+3.3	+3.3
Freq (GHz)	2.2	5	5
Reference Clock (MHz)	100	300	100
PLL Bandwidth	3.0	2.5	2.5
Power (mW)	4.2	3.6	3.0
Area (mm)	0.15	0.25	0.20

Source: own elaboration.

4. CONCLUSIONS

Thus, the design and implementation of memristor based PLL circuit is successfully implemented and testing Validation of the same is done through oscilloscope. The tunable memristor varies depends on the variable digital inputs according to the tunable input the oscillation is keep on synthesize and emulate the normalized stable PLL Clock as output.

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The future extension of the proposed work would be improved by replacing the DPLL with DDS Digital Data synthesizer, henceforth the synthesizer is further we call as MEMRISTIVE DDS.

REFERENCES

Abdalla, H., & Pickett, M. D. (2011). SPICE modeling of memristors. In *2011 IEEE International Symposium of Circuits and Systems (ISCAS)*. https://ieeexplore.ieee.org/document/5937942

Alibart, F., Gao, L., Hoskins, B. D., & Strukov, D. B. (2012). High precision tuning of state for memristive devices by adaptable variation-tolerant algorithm. *Nanotechnology, 23*(7), 075201. https://iopscience.iop.org/article/10.1088/0957-4484/23/7/075201/meta

Amarú, L., Gaillardon, P.-E., & Micheli, G. de. (2014). Majority-inverter graph: A novel data-structure and algorithms for efficient logic optimization. In *2014 51st ACM/EDAC/IEEE Design Automation Conference (DAC)*. https://ieeexplore.ieee.org/document/6881521

Borghetti, J., Snider, G., Kuekes, P., Yang, J. J., Stewart, D. R., & Williams, R. S. (2010). 'Memristive' switches enable 'stateful' logic operations via material implication. *Nature, 464*(7290), 873-876. https://doi.org/10.1038/nature08940

Chen, B., Cai, F., Zhou, J., Ma, W., Sheridan, P., & Lu, W. D. (2015). Efficient in-memory computing architecture based on crossbar arrays. In *2015 IEEE International Electron Devices Meeting (IEDM)*. https://ieeexplore.ieee.org/document/7409720

Chua, L. (1971). Memristor-the missing circuit element. *IEEE Transactions on Circuit Theory, 18*(5), 507-519. https://ieeexplore.ieee.org/document/1083337

Duan, S., Hu, X., Wang, L., Li, C., & Mazumder, P. (2012). Memristor-based RRAM with applications. *Science China Information Sciences, 55*(6), 1446-1460. https://doi.org/10.1007/s11432-012-4572-0

https://doi.org/10.17993/3ctecno.2021.specialissue8.553-565

Hu, X. F., Duan, S. K., Wang, L. D., & Liao, X. F. (2012). Memristive crossbar array with applications in image processing. *Science China Information Sciences, 55*(2), 461-472. https://link.springer.com/article/10.1007%2Fs11432-011-4410-9

Jo, S. H., Chang, T., Ebong, I., Bhadviya, B. B., Mazumder, P., & Lu, W. (2010). Nanoscale memristor device as synapse in neuromorphic systems. *Nano Letters, 10*(4), 1297-1301. https://pubs.acs.org/doi/pdf/10.1021/nl904092h

Katinsky, S., Belousov, D., Liman, S., Satat, G., Wald, N., Friedman, E. G., Kolodny, A., & Weiser, U. C. (2014). MAGIC—Memristor-aided Logic. *IEEE Transactions on Circuits and Systems II: Express Briefs, 61*(11), 895-899. https://ieeexplore.ieee.org/document/6895258

Kvatinsky, S., Friedman, E. G., Kolodny, A., & Weiser, U. C. (2013). TEAM: Threshold adaptive memristor model. *IEEE Transactions on Circuits and Systems I: Regular Papers, 60*(1), 211-221. https://ieeexplore.ieee.org/document/6353604

Lee, W. H., & Mazumder, P. (2008). Motion detection by quantum-dots-based velocity-tuned filter. *IEEE Transactions on Nanotechnology, 7*(3), 357-362. https://ieeexplore.ieee.org/document/4420105

Li, S. R., Mazumder, P., & Chua, L. (2004). Cellular neural/nonlinear networks using resonant tunneling diode. In *4th IEEE Conference on Nanotechnology.* https://doi.org/10.1002/cta.172

Pickett, M. D., Strukov, D. B., Borghetti, J. L., Yang, J. J., Snider, G. S., Stewart, D. R., & Williams, R. S. (2009). Switching dynamics in titanium dioxide memristive devices. *Journal of Applied Physics,106*(074508). https://doi.org/10.1063/1.3236506

Shilpa, V. J., & Jawahar, P. K. (2019). Cognitive Adaptive Travelling Window Filter Technology Implementation on Heterogeneous Multi-core Architecture. *International Journal of Clinical and Health Psychology, 13*.

Shilpa, V. J., Jawahar, P. K., & Karthik, S. (2018). Design of Hybrid CPU-FPGA Processor For High Performance Applications. *International Journal of Pure and Applied*

Mathematics, 119(15), 1047-1052. https://acadpubl.eu/hub/2018-119-15/3/527.pdf

Shirinzadeh, S., Soeken, M., Gaillardon, P.-E. & Drechsler, R. (2016). Fast logic synthesis for RRAM-based in-memory computing using majority-inverter graphs. In *2016 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. https://ieeexplore.ieee.org/document/7459444

Strukov, D., Snider, G., Stewart, D., & Williams, R. S. (2008). The missing memristor found. *Nature, 453*(7), 80-83. https://doi.org/10.1038/nature06932

Testa, E., Soeken, M., Zografos, O., Amaru, L., Raghavan, P., Lauwereins, R., Gaillardon, P.-E., & Micheli, G. de. (2016). Inversion optimization in majority-inverter graphs. In *2016 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*. https://ieeexplore.ieee.org/document/7568618

Wang, Z.-R., Su, Y. T., Li, Y., Zhou, Y.-X., Chu, T.-J., Chang, K.-C., Chang, T.-C., Tsai, T.-M., Sze, S. M., & Miao, X.-S. (2017). Functionally complete Boolean logic in 1T1R resistive random access memory. *IEEE Electron Device Letters, 38*(2), 179-182. https://ieeexplore.ieee.org/document/7801115

Williams, R. S. (2008). How we found the missing memristor. *IEEE Spectrum, 45*(12), 28-35. https://ieeexplore.ieee.org/document/4687366