IMPROVED RESULT OF TSV AND SLEW AWARE 3D GATED CLOCK TREE SYNTHESIS USING CHARGE RECYCLING CONFIGURATION

R. Rajalakshmi
Assistant Professor, ECE Department, Kalasalingam Institute of Technology. Krishnankoil, (India).
E-mail: rajeemtech@gmail.com
ORCID: https://orcid.org/0000-0003-1582-3600

S. M. Ramesh
Professor, ECE Department, KPR Institute of Engineering and Technology, Coimbatore, (India).
E-mail: drsmramesh@gmail.com
ORCID: https://orcid.org/0000-0003-0890-1770

P. Sivakumar
Professor, ECE Department, Kalasalingam Academy of Research and Education (Deemed to be University). Krishnankoil, (India).
E-mail: siva@klu.ac.in
ORCID: https://orcid.org/0000-0003-1328-8093

Recepción: 29/11/2019 **Aceptación:** 24/02/2021 **Publicación:** 30/11/2021

Citación sugerida:
Rajalakshmi, R., Ramesh, S. M., y Sivakumar, P. (2021). Improved result of TSV and Slew aware 3D Gated Clock Tree Synthesis using charge recycling configuration. *3C Tecnología. Glosas de innovación aplicadas a la pyme, Edición Especial,* (noviembre, 2021), 667-687. https://doi.org/10.17993/3ctecno.2021.specialissue8.667-687

ABSTRACT

In physical design of Integrated Circuits (ICs) especially after placement, Clock Tree Synthesis (CTS) plays a major part in the general chip efficiency. Three Dimensional Integrated Circuits (3D ICs) based on Through Silicon Via (TSV) present a major challenge for IC developers. 3D gated CTS on the TSV-TSV coupling model is an effective approach to reduce power, delay and clock skew. This paper proposes a slew aware TSV arrangement with clock gating logic in 3D CTS. It consists of the following 3 phases, viz., TSV clock tree synthesis, gated logic insertion in 3D CTS and charge recycling configuration for power gating structures. Unlike the previous methods available in literature, the proposed TSV aware 3D clock tree synthesis performs with TSV model in the beginning followed by the gated logic. Multiple experiments were conducted on the bench mark circuits and it can be inferred that, compared with the existing 3D CTS method on TSV-TSV coupling model, the proposed 3D gated CTS method on TSV model is simple and efficient for practical applications achieving average reduction in the clock skew and power.

KEYWORDS

3D Clock Tree Synthesis, Through-Silicon Via, 3DGated Logic, Clock Skew, Slew rate.

https://doi.org/10.17993/3ctecno.2021.specialissue8.667-687

1. INTRODUCTION

Nowadays, 3D physical design is a predominant solution in high performance computing systems. Designers have the ability to accomplish a significant number of benefits towards utilizing TSVs, for example, shorter wire length, minimum wire delay, less power and smaller chip area. TSV is a vertical electrical interconnection passing through silicon. For short interconnected length and smaller package size TSV is most important in 3D ICs. To design a high-performance clock tree, the buffer size and selection of buffer are the most dominant factors because clock distribution network determines the clock skew. The difference between the clock buffer output and the clock element inputs on the integrated circuit is called clock skew. Clock skew arises from the interconnected delays due to load mismatch. The clock skew is a significant determinant of the clock period. In order to reduce the skew due to interconnect delays, selection of buffer size is an effective way. In order to optimize the power, clock gating logic is an important consideration in the performance of digital system. Clock gating technique is not only responsible for reducing the power but also for reducing unwanted switching on the clock nets. Uncertainties in the clock timing lead to the failure of the system.

2. LITERATURE SURVEY

Burkis (1991) discussed clock tree levels, clock tree balancing effects between nodes and wire lengths during design to balance links in a buffer allocation and branch balancing techniques using only the higher number of buffers. Cirit (1990) has introduced algorithms to achieve an optimized clock allocation system for a standard cell design scheme that focuses on clock skew removal in CMOS VLSI. Chung and Cheng (1994) has implemented an algorithm called Optimal Buffer Tree Synthesis (OBTS) for minimizing the skew and propagation delay based on wire width using the dynamic programming approach.

In Menezes *et al.* (1993), and Pullela *et al.* (1993), focused only on skew reduction. The wire widening algorithm is described in Menezes *et al.* (1993) and the approach specified is based on the variation of width and length of the wires for achieving clock skew reduction. They focused and worked only on binary tree clock nets. In Pullela *et al.* (1993), by using the buffer insertion algorithm skew, delay and reduction in power are achieved on average value. In

https://doi.org/10.17993/3ctecno.2021.specialissue8.667-687

Mehta *et al.* (1997), it was shown that the significant skew is reduced by using the clustering algorithm.

Shen *et al.* (2007) provided a low-powered gated clock tree algorithm by drawing registers with comparable activity patterns, not focused on minimizing wire length, skew improvement. Li and Shi (2005) proposed and presented an algorithm for optimum buffer insertion in $O(bn^2)$ time (fast buffer insertion) as compared to $O(b^2n^2)$ algorithm, that is the extension of $O(b^2n^2)$ algorithm (Lillis, Cheng & Lin 1996), and Shi and Li (2005) has presented and proposed the algorithm for optimization of buffer insertion.

In Li and Shi (2005), and Lillis *et al.* (1996), major importance was given to make the algorithm for fast buffer insertion and the buffer cost minimization. In Yu, Dong and Chen (2010) clock tree synthesis is performed with aggressive buffer insertion, for that, Yu *et al.* (2010) proposed a clock tree routing algorithm based on maze routing to achieve robust slew control maintained with reasonable skew. Sharma (2012), in his work attempts to minimize the clock tree power and area by using 3 different cells, i.e., flip-flop based cell, gate-based cell and latch based cell.

Flip-flop is used as a control component in a flip-flop-based cell. The gate-based clock gating cell is one of the easiest cells to generate a clock gating cell in the layout compared to the flip-flop-based clock gating cell. Latch is used as a control component in latch-based clock gating. Shang *et al.* (2013) introduced electrical thermal model for reducing the clock skew by using a nonlinear programming algorithm and the results were compared with linear model and they have proved that 11.6% clock skew has been reduced and efforts have been made to improve skew minimization in CTS using nonlinear model.

Vittal and Sadowska (1997) discussed the low-power efficient design of the clock tree and created an algorithm designing the topology of the tree and inserting the buffer at the same time. They focused primarily on minimizing power. Lu, Chow and Sham (2012) presented Power Aware Clock Tree Synthesizer (PACTS) and Power and Slew Aware Clock Tree Synthesizer (PSACTS) to achieve rapid power and slew requirements while using buffer insertion and clock gates to construct the clock tree. Clock skew and power optimization is the recent crucial research topic.

https://doi.org/10.17993/3ctecno.2021.specialissue8.667-687

TSV management plays the crucial role in 3D ICs, because TSVs occupy several areas. TSVs are mainly used for connecting the different dies in physical design of VLSI circuits. Pathak *et al.* (2010) demonstrated a method for controlling the number of TSVs in 3D ICs for improving the performance and examined 3D min-cut scheme for determining the number 3D nets and proposed a change in physical design flow for determining the location of TSVs.

It is focused only on managing TSVs for reducing silicon area and not on obstacle aware. Zhao and Lim (2012) proposed TSV obstacle aware Deferred Merge Embedding (DME) technique only for avoiding TSV induced obstacles in clock routing. Kim and Kim (2011) proposed Deferred Layer Embedding (DLE)-3D Algorithm for reducing the TSV cost in 3D ICs and DME-3D Algorithm for minimizing the wire length space in 3D ICs and 3D topology algorithmNN-3D (Nearest Neighbour selection for 3D ICs) for the construction of cost effective Clock tree. The work has been made for improving cost effective clock tree generation. Cai, Deng and Zhou (2014) developed obstacle aware algorithm for the generation of clock tree and worked with buffer insertion for slew constrained and the avoidance of obstacle in clock tree synthesis.

Chao *et al.* (1992) developed the DME algorithm for reducing wire length, skew and delay in linear delay model. Most of the previous research works are related to obtaining zero skew. Only few of the recent research works are concentrated on the wire length and delay minimization achievements during clock tree synthesis. As contradicted on various meets desires once skew additionally delay minimization, there are very few meets desires accounted on skew and delay regardless of its significance. Since the clock tree synthesis is large, Often, 3D power gating logic is used to maintain an acceptable Slew rate. Kazeruni *et al.* (2013) invented the SPECO-Stochastic Perturbation based clock optimization algorithm for robust clock-tree synthesis. During clock tree synthesis, significant temperature uncertainty can occur, and it is reduced by using SPECO algorithm. SPECO algorithm has the ability to reduce the clock skew and its variance with minimized wire length overhead. Compared with DME algorithm, they have proved that their SPECO algorithm reduces clock skew and wire length overhead.

https://doi.org/10.17993/3ctecno.2021.specialissue8.667-687

Joo and Kim (2017) has proposed the polarity assignment technique for reducing the clock skew and noise moderately. This approach is applicable for reducing the clock noise especially for designing the high-speed system with rigid time margin. Li *et al.* (2008) have developed and patented the method for identifying clock entry points for each partition to perform clock tree synthesis at top level and then created virtual leaf points for grids to determine the clock skew and latency.

Lai *et al.* (2007) suggested and patented the method for obtaining synthesis of the low power clock tree by using buffer insertion, resizing and removal technique for the VLSI circuits. Lin *et al.* (2016) have proposed 3D gated CTS for achieving slew rate, minimization of skew and low power consumption. Liu *et al.* (2013) have proposed 3D CTS for mitigating the effect of TSV-TSV coupling and for reducing power consumption. Lu and Srivastava (2017) have developed K-means clustering based algorithm for low power CTS for 3D ICs and achieved better power savings. In almost all of the previous works, designers concentrated to reduce the clock skew, power, wire delay by using buffer insertion, relocation, resizing and removal technique with TSV for 3D ICs. But in this work, gated logic power gated method and charge recycling technique are proposed for power gated structures with TSV in 3D ICs for achieving low power and to reduce the skew.

3. IMPORTANCE OF CTS IN 3D ICS

In this section, the importance of clock tree synthesis, the effect of TSV on 3D integrated circuits and skew reduction are first discussed and then power gating logic is inserted into TSV model to reduce the power consumption. In physical design, CTS plays a major part in the chip's overall performance, particularly after placement.3D clock tree synthesis with gated logic is the powerful approach to minimize the power. In 3D clock tree synthesis, clock gating logic and clock skew are the most important factors in layout strategy. To create high performance clock network, control and power optimization, clock gating logic is an important consideration in the performance of digital system.

https://doi.org/10.17993/3ctecno.2021.specialissue8.667-687

3.1. PRELIMINARIES AND PROBLEM FORMULATION

TSV model of 3D clock network

Figure1 shows the TSV between the dies 1, 2 and 3. This is the modified figure of (Liu et. al 2015) TSV between different Dies. Fig.1 illustrates die (1), Die (2), up to die (N−1) for N die stacked 3D design in a top-down way where the die at the source of the clock is called as the source die. TSV is comprised of several TSVs between neighbouring dies between nonadjacent dies. Here we modelled the TSV 3D clock network with the coupling impact of TSV-to-TSV.

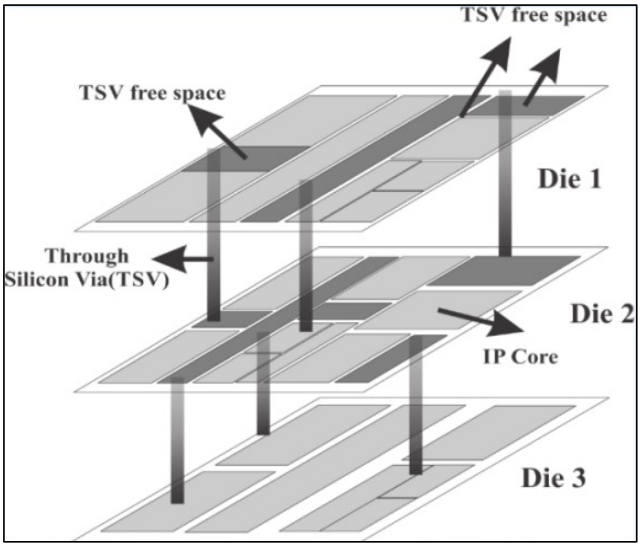

Figure 1. TSV between Die1, Die2 and Die3.
Source: own elaboration.

In 3D clock tree synthesis coupling effect between TSVs is significant because it leads to extra power and delay. For evaluating the impact of TSVs on 3D CTS, TSV-TSV coupling model is adopted (Liu *et al.*, 2015). Figure 2 shows TSV coupling model.

https://doi.org/10.17993/3ctecno.2021.specialissue8.667-687

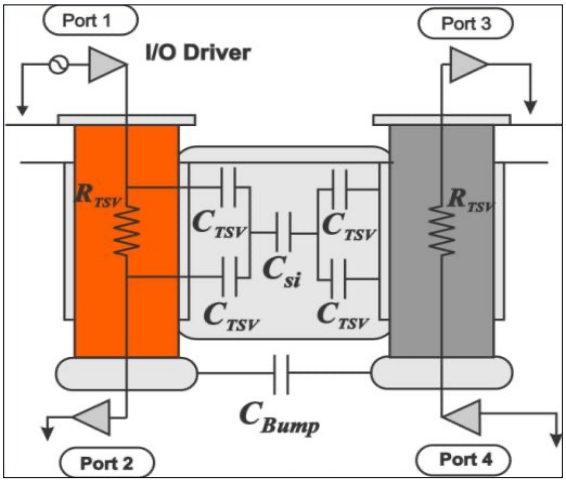

Figure 2. TSV-TSV coupling model.
Source: own elaboration.

The following formula (Liu *et al.*, 2015) are adopted and used for the calculation of resistances and capacitances, where ε_r is the relative permittivity and ε_0 is the dielectric constant of vacuum and. r_{TSV} is the radius of TSV and l_{TSV} is the height of TSV, t_{ox} is the thickness of the insulator.

$$R_{TSV} = \frac{l_{TSV}}{\sigma \pi r_{TSV}^2} \tag{1}$$

$$C_{TSV} = \frac{1}{4} \frac{2\pi \varepsilon_0 \varepsilon_r}{1n\left(\frac{r_{TSV} + t_{OX}}{r_{TSV}}\right)} \times l_{TSV} \tag{2}$$

$$C_{si} = \varepsilon_0 \varepsilon_{si} \frac{2(r_{TSV} + t_{OX}) + \alpha}{d} \times l_{TSV} \tag{3}$$

$$C_{Bump} = \frac{\varepsilon_0 \varepsilon_r}{d - 2_{rBump}} \times \pi \times r_{Bump} \times l_{Bump} \tag{4}$$

where ε_0 and ε_{si} are the dielectric constant of vacuum and silicon, α is the scaling factor, r_{TSV} and l_{TSV} are the TSV radius and height, r_{Bump} and l_{Bump} are the radius and the height of a bump, t_{OX} is the thickness of the insulator, and d is the distance between two TSVs.

https://doi.org/10.17993/3ctecno.2021.specialissue8.667-687

Where ε_0 and ε_{si} are vacuum and silicon dielectric constants, α is the scaling factor, r_{TSV} and l_{TSV} are the TSV radius and height, r_{Bump} and l_{Bump} are the radius and height of the bump, t_{OX} is the insulator thickness and d is the distance between two TSVs.

Here the pulse signal is applied to one TSV which will act as a source circuit while the other TSV will act as a victim circuit. Simulation of this equivalent circuit model is done by the Microwind simulator using the parameters specified in Liu *et al.* (2015).

4. PROPOSED METHOD

Slew Aware 3D Gated Clock Tree Synthesis

We have proposed TSV-TSV coupling model (Liu *et al.*, 2015) with clock gating logic (Shen *et al.*, 2010) for improving power consumption and slew rate.

Figure 3 shows TSV-TSV coupling model with clock gating logic and Figure 4 shows the clock gating logic for 3D-CTS.

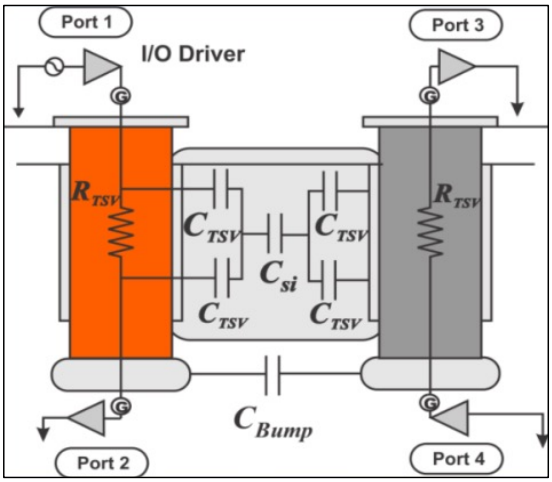

Figure 3. TSV-TSV coupling model with clock gating logic.
Source: own elaboration.

https://doi.org/10.17993/3ctecno.2021.specialissue8.667-687

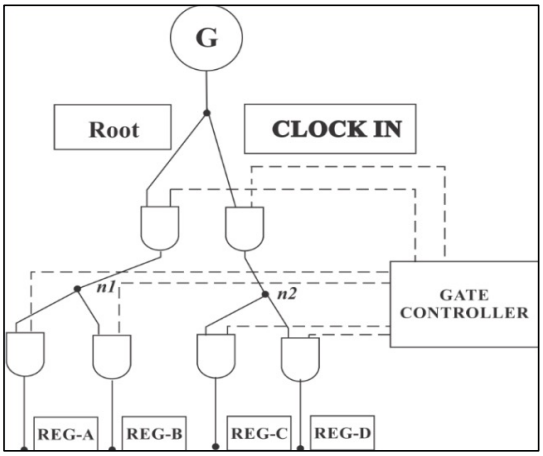

Figure 4. Clock gating logic for 3D CTS.
Source: own elaboration.

Here, the Gate controller is located in the centre. n1 and n2 specifies the nodes of the clock gating logic and each edge of Gate controller tree is considered as ENi, which controls the gate on each edge.

4.1. PROCESS FLOW OF SLEW AWARE 3D GATED CTS

As specified in the recent research, the number and areas of TSVs are essential and only a small number of slew aware blocks are accessible in 3-D CTS for clock TSVs. None of the current strategies still work effectively in this situation. Here, a TSV-TSV coupling model with clock gating logic in 3-D CTS is proposed with charge recycling configuration for power gating structure is used. Figure 5 shows Slew aware 3D gated CTS process flow. This is the modified process flow. Liu *et al.* (2015) proposed white space aware 3D CTS Process flow. Here slew aware CTS process is developed.

https://doi.org/10.17993/3ctecno.2021.specialissue8.667-687

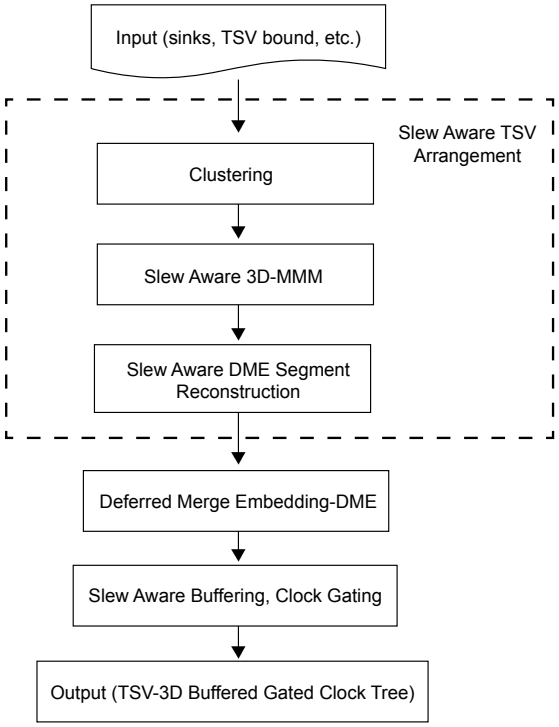

Figure 5. Slew aware 3D gated CTS process flow.
Source: own elaboration.

The proposed method's process flow is specified as follows.

1. Formulation of Slew aware TSV adaption in 3D gated CTS and 3D-MMM algorithm to solve the problem.

2. 3D-MMM Algorithm comprises 3 phases namely:

   a. Slew aware sink pre-clustering, which distributes the sinks to neighbouring skew blocks.

   b. TSV and slew aware clock tree generation, this means that every sink set includes skewed blocks.

   c. Slew aware Reconstruction of the DME segment for easy routing and TSV arrangement.

3. Unlike previous 3-D CTS approaches that enhance the TSV as shown by 2C-R demonstrate, the TSV-TSV coupling model with gated logic in 3D CTS is proposed

https://doi.org/10.17993/3ctecno.2021.specialissue8.667-687

and used to assess the TSV coupling impacts, and a clock gating logic strategy is used to ease the TSV-TSV coupling impacts.

4. Exploration of relationship among TSV, slew aware area and slew rate, power and clock skew is clearly differentiated in this proposed method using 3D-MMM CTS. The 3D Gated CTS method is applied to the standard ISPD benchmarks circuits (ISPD09F11, ISPD09F12, ISPD09F21, ISPD09F22, ISPD09F33 and ISPD09F35).

Clustering:

Because the TSV insertion clock skew blocks are very small, the sinks of the clock are distributed. Ignoring the skew blocks during 3D CTS with TSVs would lead to clock skew increase and wire length overhead.

To reduce this issue, sink pre-clustering method is introduced as given in Liu *et al.* (2015). For each cluster, by using MMMs (Mean and Medians) and DME, sub tree is generated for detailed routing and clock tree topology generation. TSV-to-TSV Coupling Model and the hierarchy of 3D Clock Tree is shown in the following figures Figure 6 and Figure 7.

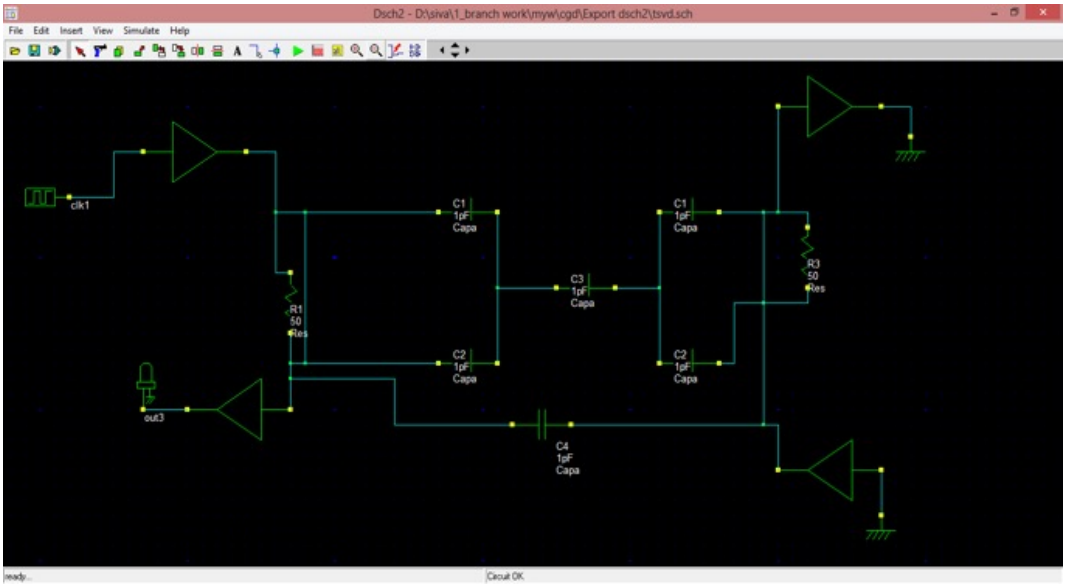

Figure 6. TSV-to-TSV Coupling Model.
Source: own elaboration.

https://doi.org/10.17993/3ctecno.2021.specialissue8.667-687

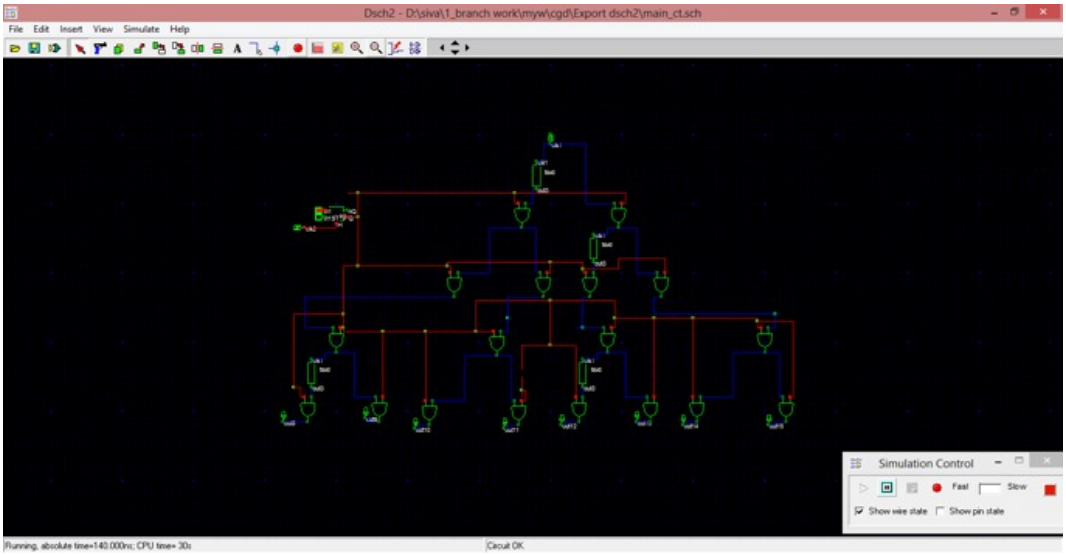

Figure 7. The hierarchy of 3D Clock Tree.
Source: own elaboration.

TSV Slew Aware 3D-MMM and Slew aware DME segment Reconstruction:

TSV Slew aware 3D-MMM algorithm first divides the sinks into two subsets and proceeds until each sink belongs to its own set. There are two levels available in the DME segment method (Liu *et al.*, 2015), namely the Bottom up level and the Top down level. Bottom up level calculates all combined sub-trees locations. These internal nodes are embedded in the top-down level.

Slew aware Buffering:

In 3D CTS, Slew rate control is most important because high slew rate can cause power consumption to be high. For ensuring this, two types of buffers are inserted to control the slew rate. One is Clock buffer that is inserted along the wire and another one is TSV buffer that is inserted at each node for testability. After clock routing, slew aware buffering is done to attain the o(n) computational complexity.

Power Gating:

Appropriate power gating structure design (e.g. multi-threshold CMOS (MTCMOS) or super-cut-off CMOS) is an important and challenging task in sub-90 nm VLSI circuits

https://doi.org/10.17993/3ctecno.2021.specialissue8.667-687

with significant leakage currents. A major quantity of energy is consumed in designs where mode transitions are common to switch on or off the power gating structure. Developing a power gating option that minimizes the energy consumed during mode transitions is therefore desirable. Here the charge recycling configuration (Pakbaznia, Fallah, & Pedram, 2006) for power gating structure is adopted and used as shown in Figure 8.

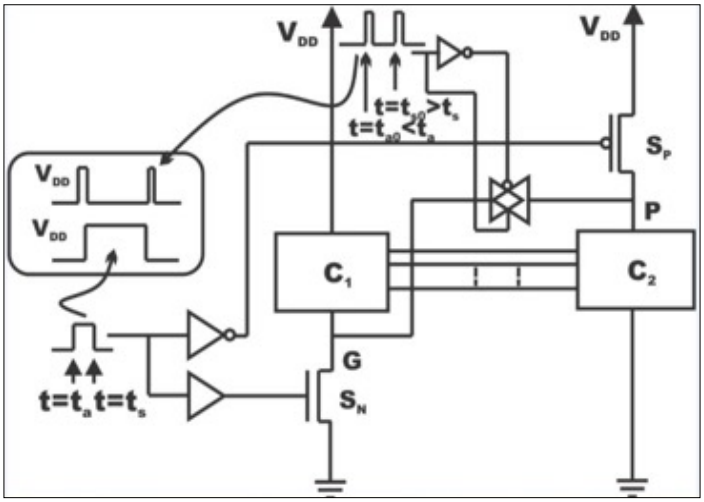

Figure 8. Charge-recycling configuration for power gating structures.
Source*:* own elaboration.

Energy Saving by Charge Recycling:

At the beginning, it should be stated that for the purpose of analyzing energy consumption in CMOS circuits, only when a capacitive node is charged via a direct connection to the VDD rail is taken out of the VDD rail.

The recycling of loads between "floating" capacitive nodes does not remove any energy from the VDD rail or dump any energy into the ground rail, but instead some of the energy stored in the inverters is accumulated in the resistance of the switch that short circuits the two capacitive nodes while the rest of the energy is properly spread between the nodes..

Two distinct transitions are classified in order to calculate the energy saving of the charge-recycling method: wake-up transition, sleep-to-active and sleep transition, active-to-sleep transition.

https://doi.org/10.17993/3ctecno.2021.specialissue8.667-687

Calculation of the energy saving Ratio (ESR) as follows:

$$\frac{E_{TG}}{E_{MTCMOS}} = \frac{2C_{tg}\,V_{DD}^2}{(C_G + C_P)V_{DD}^2} = \frac{2C_{tg}}{C_G + C_P} \quad (5)$$

where,

C_G = charge up capacitance

C_P = discharged capacitance

C_{TG} = transmission gate capacitance.

5. RESULTS

Experimental results were done by using SPICE. First, it is applied with Traditional 3D CTS method. The suite is incorporated into TSV 3D gated CTS method. Then the Levels of trees namely TSV 30 , TSV 36, TSV 42,TSV 44, TSV 89 and TSV 93 are constructed using TSV 3D MMM algorithm which is the conventional method.

3D-Gated CTS Layout Design and 3D Layout model is shown in the figures 9(a) and 9(b) respectively.

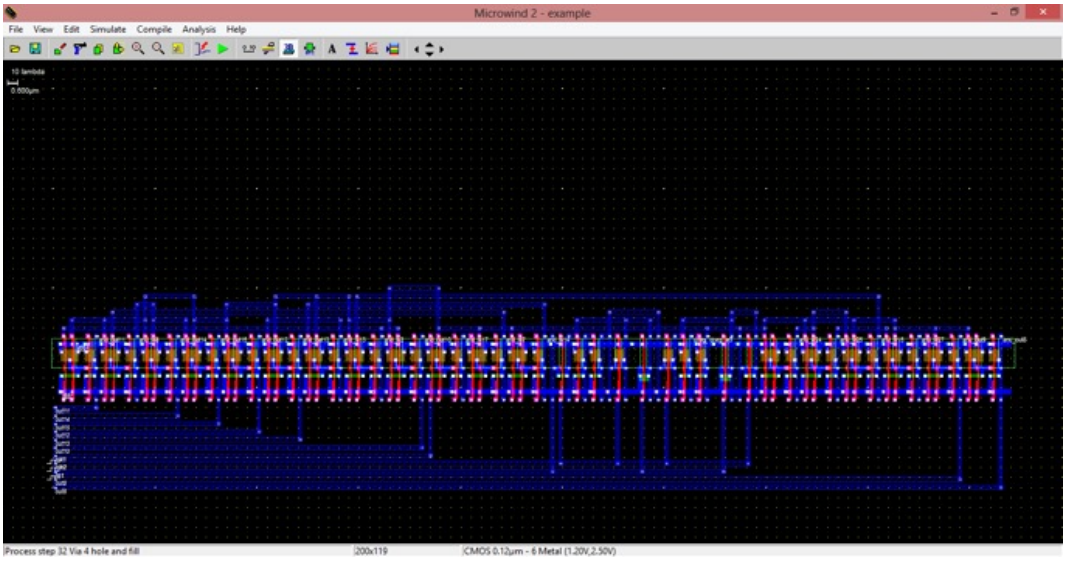

Figure 9 (a). 3D Gated CTS Layout Design.
Source: own elaboration.

https://doi.org/10.17993/3ctecno.2021.specialissue8.667-687

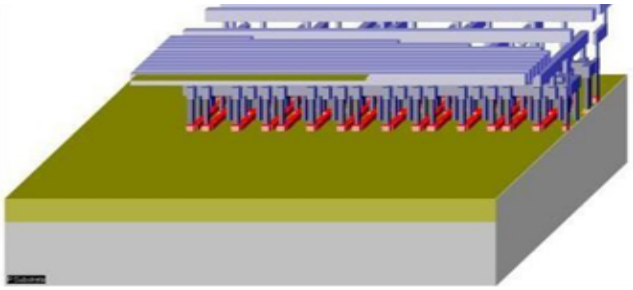

Figure 9 (b). 3D Layout model.
Source: own elaboration.

The following Figures 10(a) and 10(b) provide the comparison between the parameters used in traditional 3D CTS method and TSV 3D gated CTS method.

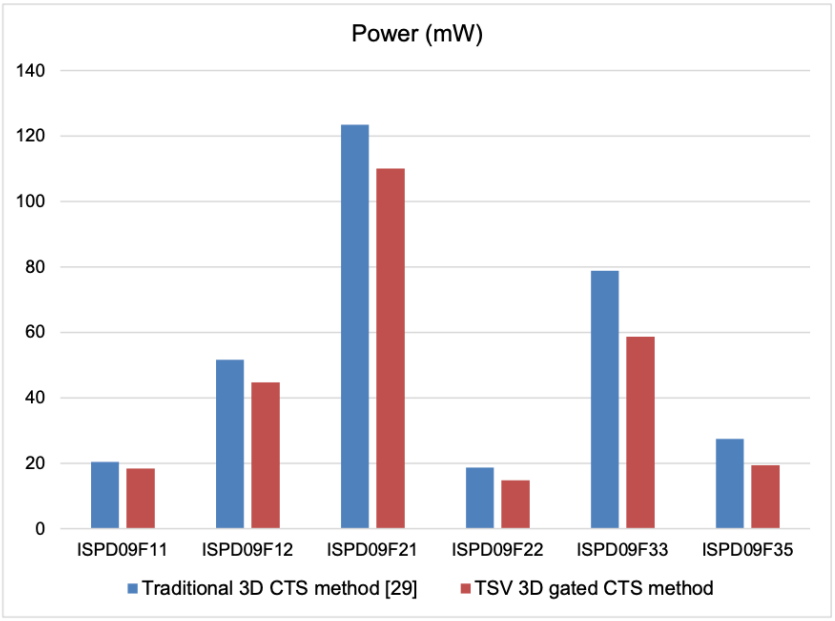

Figure 10 (a). Comparison of power for traditional 3D CTS method and TSV 3D gated CTS method.
Source: own elaboration.

https://doi.org/10.17993/3ctecno.2021.specialissue8.667-687

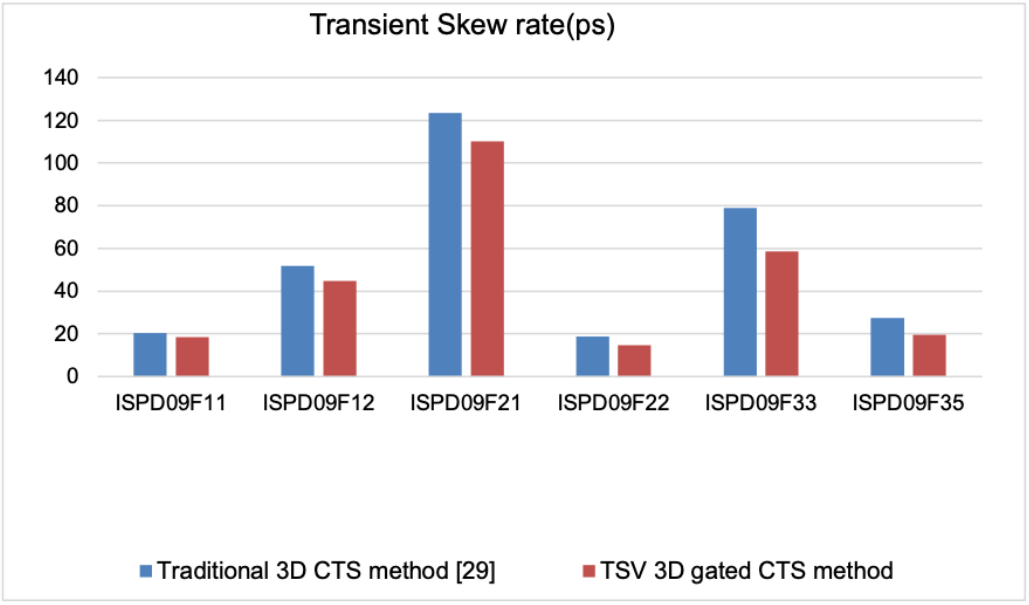

Figure 10 (b). Comparison of transient skew rate for traditional 3D CTS method and TSV 3D gated CTS method.
Source: own elaboration.

The overall result for the Benchmark suite by applying both the traditional 3D CTS method and TSV 3D gated CTS method are compared in the below Table 1.

Table 1. Comparison results of traditional 3D CTS method and TSV 3D gated CTS method.

	Traditional 3D CTS method			TSV 3D gated CTS method			Energy saving by using charge recycling configuration
Benchmark	**N_ TSV**	**Power (mW)**	**Transient Skew rate (ps)**	**N_ TSV**	**Power (mW)**	**Transient Skew rate (ps)**	
ISPD09F11	56	20.36	17.87	30	18.38	16.68	43%
ISPD09F12	71	51.69	11.25	36	44.86	12.13	41%
ISPD09F21	39	123.4	23.86	42	110.1	22.65	42%
ISPD09F22	82	18.71	12.45	44	14.69	13.39	40%
ISPD09F33	94	78.87	15.67	89	58.72	15.48	44%
ISPD09F35	85	27.53	13.24	93	19.43	12.94	45%

Source: own elaboration.

https://doi.org/10.17993/3ctecno.2021.specialissue8.667-687

6. CONCLUSIONS

In this proposed work, the practical skew issue in TSV and slew aware gated Clock Tree Synthesis for 3D IC's is addressed. TSV-TSV coupling effects with 3D-MMM algorithm and slew aware gated CTS are concentrated mainly. The most important element that influences the effectiveness of traditional calculations on 3D gated CTS is the clock skew. Therefore, maximum efforts are taken in eliminating the negative effect on clock skew along with slew rate and power. TSV-TSV coupling model with clock gating logic insertion has been developed in 3D CTS. Owing to the results presented in table 1, it is clear that the suggested TSV Gated technique significantly reduced power and transient skew rate compared to the conventional TSV method. On the whole, the average power and the average transient skew rate attained using the proposed method are $1.51e^2$ times and 1.25 times, respectively lesser than those attained using the conventional method. Hence the proposed 3D Gated CTS method proves to be effective in reducing power and transient skew rate.

7.REFERENCES

Burkis, J. (1991). Clock tree synthesis for high performance ASICs. *Proceedings Fourth Annual IEEE International ASIC Conference and Exhibit*, pp. P9-8/1. https://doi.org/10.1109/ASIC.1991.242921

Cai, Y., Deng, C., & Zhou, Q. (2014). Obstacle-Avoiding and Slew-Constrained Clock Tree Synthesis With Efficient Buffer Insertion. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 23*(1), 142-155. https://doi.org/10.1109/TVLSI.2014.2300174

Chao, T.-H., Hsu, Y.-C., Ho, J.-M., & Boese, K. D. (1992). Zero skew clock routing with minimum wirelength. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, 39*(11), 799-814. https://doi.org/10.1109/82.204128

Chung, J., & Cheng, C. K. (1994). Optimal buffered clock tree synthesis. *Proceedings Seventh Annual IEEE International ASIC Conference and Exhibit*, pp. 130-133. https://doi.org/10.1109/ASIC.1994.404593

https://doi.org/10.17993/3ctecno.2021.specialissue8.667-687

Cirit, M. A. (1990). Clock skew elimination in CMOS VLSI. In *IEEE International Symposium on Circuits and Systems,* 861-864 vol. 2. https://doi.org/10.1109/ISCAS.1990.112222

Joo, D., & Kim, T. (2017). Clock buffer polarity assignment under useful skew constraints, *Integration, 57*, 52-61. https://doi.org/10.1016/j.vlsi.2016.11.007

Kazeruni, S. B., Yu, H., Gong, F., Hu, Y., Liu, C., & He., L. (2013). SPECO: Stochastic Perturbation based Clock tree Optimization considering temperature uncertainty. *Integration, 46*(1), 22-23. https://doi.org/10.1016/j.vlsi.2012.04.004

Kim, T.Y., & Kim, T. (2011). Clock Tree Synthesis for TSV-Based 3D- IC Designs. *ACM Transactions on Design Automation of Electronic Systems, 16*(4). https://doi.org/10.1145/2003695.2003708

Lai, M.-H., Chang, C.-K., Chu, C.-C., & Feng, W.-S. (2007). Clock Tree Synthesis for Low power Consumption and Low clock skew. *US Patent,* US 7, 216, 322 B2, May 8. https://patents.google.com/patent/US7216322B2/en

Li, H.-C., Kuo, C.-C., Lai, M., & Chen, M.-C. (2008). Method and system for Clock Tree Synthesis of an integrated circuit. *US Patent*, US 7, 467, 367 B1, Dec. 16. https://patents.google.com/patent/US7467367

Li, Z., & Shi, W. (2005). An O(bn²) Time algorithm for optimal buffer insertion with b Buffer types. In *Dans Design, Automation and Test in Europe - DATE'05*. https://arxiv.org/abs/0710.4691

Lillis, J., Cheng, C.-K., & Lin, T.Y. (1996). Optimal wire sizing and buffer insertion for low power and a generalized delay model. *IEEE Journal of Solid-State Circuits, 31*(3), 437-447. https://doi.org/10.1109/4.494206

Lin, M., Sun, H., & Kimura, S. (2016). Power-efficient and slew-aware three dimensional gated clock tree synthesis. In *2016 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, pp. 1-6. https://doi.org/10.1109/VLSI-SoC.2016.7753535

Liu, W., Du, H., Wang, Y., Ma, Y., Xie, Y., Quan. J., & Yang, H. (2013). TSV-aware topology generation for 3D Clock Tree Synthesis. *In International Symposium*

on Quality Electronic Design (ISQED), pp. 300-307. https://doi.org/10.1109/ISQED.2013.6523626

Liu, W., Wang, Y., Chen, G., Ma, Y., Xie, Y., & Yang, H. (2015). Whitespace-Aware TSV Arrangement in 3-D Clock Tree Synthesis. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 23*(9), 1842-1853. https://doi.org/10.1109/TVLSI.2014.2354347

Lu, J., Chow, W. K., & Sham, C. W. (2012). Fast Power- and Slew-Aware Gated Clock Tree Synthesis. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 20*(11), 2094-2103. https://doi.org/10.1109/TVLSI.2011.2168834

Lu, T., & Srivastava, A. (2017). Low power Clock Tree Synthesis for 3D ICs. *ACM Transactions on Design Automation of Electronic Systems, 22*(3), 1-24. https://doi.org/10.1145/3019610

Mehta, A. D., Chen, Y.-P., Menezes, N., Wong, D.F., & Pileggi, L.T. (1997). Clustering and load balancing for buffered clock tree synthesis. *Proceedings International Conference on Computer Design VLSI in Computers and Processors*, pp. 217-223. https://doi.org/10.1109/ICCD.1997.628871

Menezes, N., Balivada, A., Pullela, S., & Pillage, L. T. (1993). Skew reduction in clock trees using wire width optimization. *Proceedings of IEEE Custom Integrated Circuits Conference - CICC '93*, pp. 9.6.1-9.6.4. https://doi.org/10.1109/CICC.1993.590684

Pakbaznia, E., Fallah, F., & Pedram, M. (2006). Charge Recycling in MTCMOS Circuits: Concept and Analysis. *DAC '06: Proceedings of the 43rd annual Design Automation Conference*. https://doi.org/10.1145/1146909.1146940

Pathak, M., Lee, Y.-J., Moon, T., & Lim, S. K. (2010). Through-silicon-via management during 3D physical design: When to add and how many? In *2010 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 387-394. https://doi.org/10.1109/ICCAD.2010.5653703

Pullela, S., Menezes, N., Omar, J., & Pillage, L. T. (1993). Skew And Delay Optimization For Reliable Buffered Clock Trees. *Proceedings of 1993 International*

Conference on Computer Aided Design (ICCAD), pp. 556-562. https://doi.org/10.1109/ICCAD.1993.580114

Shang, Y., Zhang, C., Yu, H., Tan, C.S., Zhao, X., & Lim, S. K. (2013). Thermal-reliable 3D clock-tree synthesis considering nonlinear electrical-thermal-coupled TSV model. In *2013 18th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 693-698. https://doi.org/10.1109/ASPDAC.2013.6509681

Sharma, D. K. (2012). Effects of different clock Gating Techniques on Design. *International Journal of Scientific & Engineering Research, 3*(5). https://www.ijser.org/researchpaper/Effects-of-Different-Clock-Gating-Techinques-on-Design.pdf

Shen, W., Cai, Y., Hong, X., & Hu, J. (2007). Activity-Aware Registers Placement for Low Power Gated Clock Tree Construction. *IEEE Computer Society Annual Symposium on VLSI (ISVLSI '07)*, pp. 383-388. https://doi.org/10.1109/ISVLSI.2007.20

Shen, W., Cai, Y., Hong, X., & Hu, J. (2010). An Effective Gated Clock Tree Design Based on Activity and Register Aware Placement. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 18*(12), 1639-1648. https://doi.org/10.1109/TVLSI.2009.2030156

Shi, W., & Li, Z. (2005). A fast algorithm for optimal buffer insertion. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 24*(6), 879-891. https://doi.org/10.1109/TCAD.2005.847942

Vittal, A., & Sadowska, M. M. (1997). Low-power buffered clock tree design. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 16*(9), 965-975. https://doi.org/10.1109/43.658565

Yu, Y., Dong, C., & Chen, D. (2010). Clock tree synthesis under aggressive buffer insertion. *Proceedings of the 47th Design Automation Conference,* pp. 86-89. https://doi.org/10.1145/1837274.1837297

Zhao, X., & Lim, S.K. (2012). Through-silicon-via-induced obstacle-aware clock tree synthesis for 3D ICs. In *17th Asia and South Pacific Design Automation Conference,* pp. 347-352. https://doi.org/10.1109/ASPDAC.2012.6164971